REMARKS:

Claims 1-27 were presented for examination and were pending in this application. In an Official Action dated August 8th, 2005, claims 11-15 and 18 were allowed, claims 16 and 17 were objected to, claims 1-10 were rejected, and claims 19-27 were subjected to a restriction and/or election requirement. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Applicants herein amend claims 1 and 10. Claims 19-27 are cancelled without prejudice or disclaimer. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended and/or cancelled to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments and cancelling these claims, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC 103(a) in View of Intel and Case

In the 6th paragraph of the Office Action, Examiner rejects claim 1 under 35 USC § 103(a) as allegedly being unpatentable in view of Intel's Pentium Processor Family

Developer's Manual, Vol. 3: Architecture and Programming Manual, 1995, ("Intel") and U.S. Patent No. 4,777,587 to Case et al. ("Case"). This rejection is respectfully traversed.

Claim 1, as amended, recites a method for performing arithmetic in a memory to memory architecture comprising, among other things,

> responsive to receiving the fixed length instruction:
>
> accessing, from the source address in the memory, a first operand on which the mathematical operation is to be performed;
>
> ...; and
>
> storing the result in the destination address in the memory, *wherein the destination address in the memory is different from the source address in the memory.*

(emphasis added)

As the Examiner suggested in the Office Action, Applicants have clarified this beneficial feature of the invention. By being able to specify two different memory locations as source and destination within a single fixed-length instruction, the claimed invention has the desirable capability to handle two memory operands in a single operation. This benefit is explained in the specification, for example where it describes the following:

> A processor's ability to handle two memory operands in one instruction reduces the number of instructions required to perform many functions. For instance, data can be moved from one memory location to another in a single instruction. Another example of the use of two memory operands is that data from memory can be added with data from a register and stored in memory with a single instruction. This function can be performed without the steps of loading the data to a register, performing the add, and then storing the result. The present invention serves to eliminate several of the load and store instructions inherent in RISC architecture, while still maintaining simple hardware and software.

Specification, paragraph 14.

By contrast, the Intel reference lacks this fixed-length instruction ability to specify two memory locations for a single memory to memory operation. The Intel reference simply describes the variable-length instruction set for the Pentium® processor family. As Examiner points out, the Intel reference does not show a fixed length instruction; Intel's Pentium architecture is based on a variable length instruction set. Further, the "ADD" instruction fails to show or suggest (1) "a source address in a memory," (2) "a source address in a register file," and (3) a different "destination address in the memory." The Intel reference describes that "[t]he ADD instruction performs an integer addition of the two operands (DEST and SRC). The result of the addition is assigned to the first operand (DEST), and the flags are set accordingly." Intel, p.25-29 (emphasis added). Since the result is assigned to the first operand (i.e., it is stored in the same memory location), there is no need in the Intel instruction set to specify an additional memory address, as the claim requires. In addition, the combination with Case fails to make up for this deficiency in the Intel reference. Case simply teaches that using fixed length instructions enables the instructions to be easily decoded. The Case reference does not show or suggest a fixed-length instruction capable of specifying two different memory locations as source and destination for an operand. Therefore, Intel and Case as cited do not store the result in the destination address in the memory, "wherein the destination address in memory is different from the source address in the memory."

Based on the above Amendment and the following Remarks, Applicants respectfully submit that for at least these reasons claim 1 is patentably distinguishable over the cited

references, both alone and in combination. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

As claims 2-9 are dependent on claim 1, all arguments advanced above with respect to claim 1 are hereby incorporated so as to apply to claims 2-9. Moreover, these arguments are equally applicable to the apparatus of claim 10. Claim 10 is rejected for the same reasons set forth in claim 1. Like claim 1, claim 10 is also amended to clarify that the source and destination addresses in memory are different memory locations. Accordingly, Applicants respectfully submit that claims 2-10 are also patentable over the cited references, alone and in combination. Therefore, Applicants respectfully request prompt allowance of claims 1-10.

As the amendments of claims 1 and 10 clarify, the claimed invention "[stores] the result in the destination address in the memory, wherein the destination address in memory is different from the source address in memory." Applicants respectfully submit that this clarifying amendment does not necessitate a new search since any search performed for art relating to the prior form of the claims would have yielded a superset of references that, if at all, would have included references relating to the currently amended claims. Accordingly, applicants kindly request prompt allowance of claims 1-10.

Response to Objection

In the 29th paragraph of the Office Action, the Examiner objects to claims 16 and 17 as being dependent upon a rejected base claim, but notes that they would be allowable if rewritten in independent form. However, Examiner is respectively asked to note that claims 16 and 17 depend directly or indirectly on claims allowed by the examiner, claims 15, 13,

and 11 (claim 17 depending from claim 16). Therefore applicants respectfully request Examiner to withdraw the objection.

Clarification Regarding Claim 18

In the 30th paragraph of the Office Action, the Examiner allows claims 11-15 and 18. Applicants thank the Examiner for this consideration. This action is appropriately reflected on the Office Action Summary, as claim 18 is listed among the claims that are allowed. However, on the Office Action Summary page the Examiner has also indicated that claims 18-27 are subject to restriction and/or election requirement. Applicants request clarification regarding the status of Claim 18 in light of this apparent contradiction. Furthermore, in the 1st paragraph of the Office Action, the Examiner puts claim 18 in Group I with claims 1-17, and in the 4th paragraph it is claims 19-27 that are subject to the restriction requirement. Therefore, Applicants kindly submit that the inclusion of claim 18 in the summary of claims subject to restriction and/or election is a clerical error and kindly request prompt allowance of claim 18.

Conclusion

In sum, Applicants respectfully submit that claims 1 through 18, as presented herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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Date: 26 Oct 2005 By: _____

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